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**Topic: Basic ALU Implementation using iVerilog**

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**Sub Code: 19CS211 Sub Title: COA**

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1. Design of 1 bit ALU with the following operations

**iVerilog Code:**

module alu(a, b, op, out);

input a, b;

input[2:0] op;

output out;

reg out;

always@(a or b or op)

begin

case(op)

3'b000: out=a+b;

3'b001: out=a-b;

3'b010: out=(a & b);

3'b011: out=(a | b);

3'b100: out=!a;

3'b101: out=!(a & b);

3'b110: out=!(a | b);

3'b111: out=0;

endcase

end

endmodule

**TestBench :**

module alu\_tb;

reg t\_a, t\_b;

reg [2:0] t\_op;

wire t\_out;

alu my\_alu(.op(t\_op),.a(t\_a),.b(t\_b),.out(t\_out));

initial

begin

$monitor(t\_a, t\_b, t\_out);

t\_a=1;

t\_b=0;

t\_op=3'b000;

#10

t\_a=1;

t\_b=0;

t\_op=3'b001;

#10

t\_a=1;

t\_b=0;

t\_op=3'b010;

#10

t\_a=1;

t\_b=0;

t\_op=3'b011;

#10

t\_a=1;

t\_b=0;

t\_op=3'b100;

#10

t\_a=1;

t\_b=0;

t\_op=3'b101;

#10

t\_a=1;

t\_b=0;

t\_op=3'b110;

#10

t\_a=1;

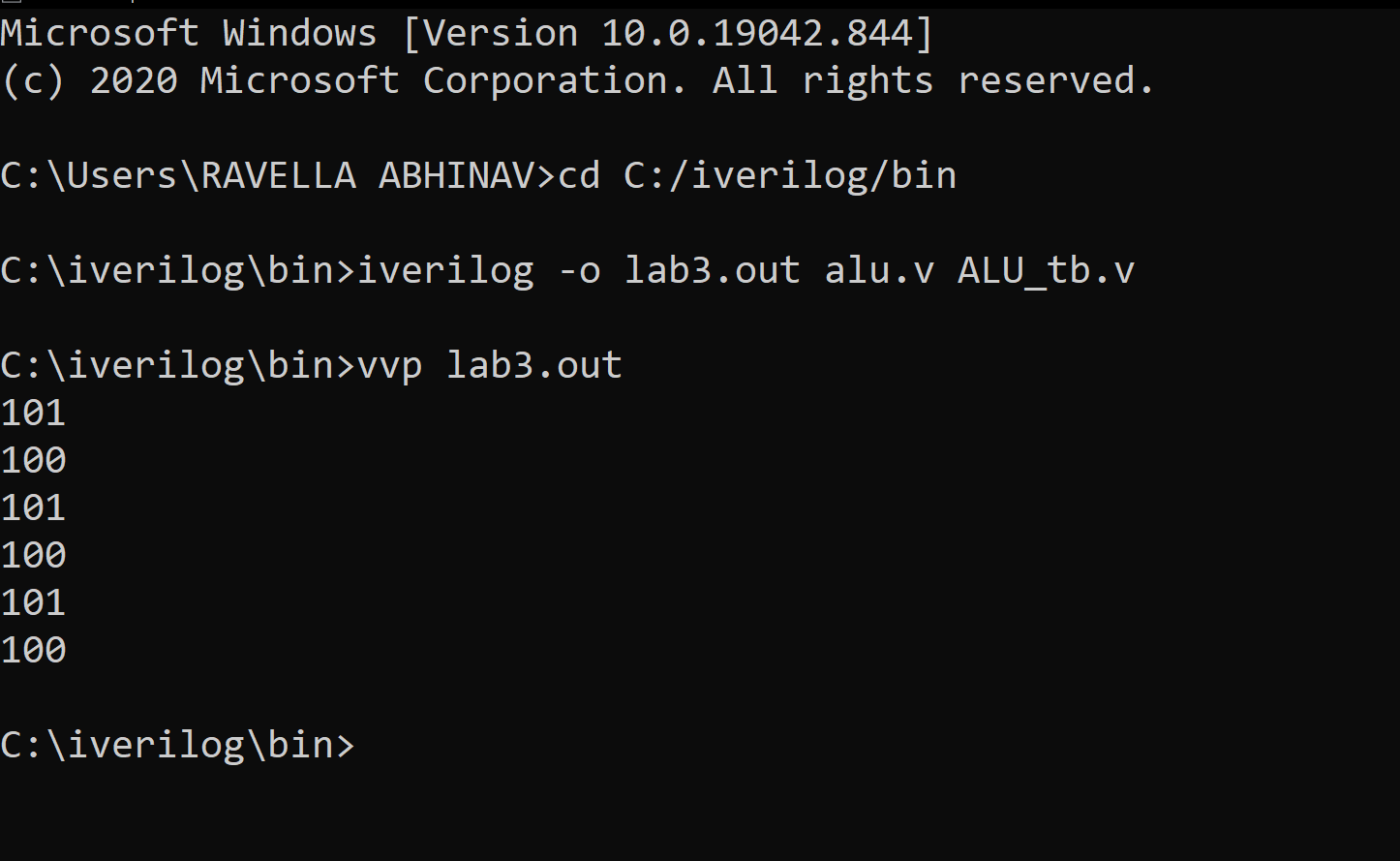
t\_b=0;

t\_op=3'b111;

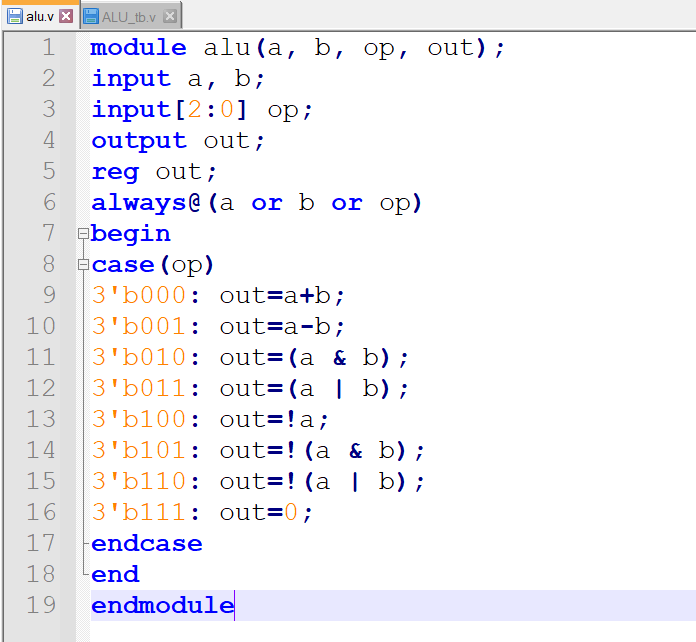
end

endmodule

**Output :**

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**Code Snippets :**

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